

CLAIMS

What is claimed is:

- 1 1. A method for providing an interconnect on a semiconductor device comprising
2 the steps of:
3 (a) providing a semiconductor substrate with a plurality of device structures
4 thereon;
5 (b) providing at least one slot in the semiconductor substrate, and
6 (c) providing a metal within the at least one slot.
7
8 2. The method of claim 1 wherein the semiconductor substrate providing step (a)
9 further comprises:
10 (a1) providing a substrate region;
11 (a2) providing an epitaxial (EPI) layer over the substrate region; and
12 (a3) etching a plurality of device structures in the EPI layer.
13
14 3. The method of claim 1 wherein the at least one slot providing step (b) includes
15 the step of (b1) oxidizing the at least one slot.
16
17 4. The method of claim 2 wherein the at least one slot providing (b) comprises (b1)
18 providing the slot to the surface of the EPI layer.
19
20 5. The method of claim 1 wherein the at least one metal providing step (c)

comprises the step of:

(c1) filling the slot utilizing a metal that is provided on the surface of the EPI layer that is of a thickness that is one-half the depth or width of the at least one slot.

6. The method of claim 1 wherein the at least one metal comprises a plurality of metals.

7. The method of claim 6 wherein the plurality of metals comprises two metals, a first metal covers one half the slot depth and a second metal fills the slot.

8. The method of claim 6 wherein the plurality of metals comprises three metals, wherein the first and second metal fill the slot and the third metal provides an interconnect layer.

9. The method of claim 3 wherein the oxide is removed from the bottom of the slot and the interconnect forms a low resistance to ground.

10. The method of claim 3 wherein a buried layer is under the slot, the oxide is removed from the bottom of the slot, and the interconnect forms a low resistance sinker.

11. The method of claim 1 wherein the at least one metal is provided utilizing chemical vapor deposition.

1 12. The method of claim 1 wherein the at least one metal is provided utilizing
2 maskless sputter depositions.

1 13. The method of claim 12 wherein the slot edges are shaped via oxidation.

1 14. The method of claim 13 wherein the slot edges are shaped via depositing a
2 photoresist on the metal and planar etching the photoresist, the metal in the field, a slight oxide
3 etch , and then removal of the resist.

15. The method of claim 14 wherein spin on glass is utilized for the planar etching.

1 16. A semiconductor device comprising:
2 a semiconductor substrate, the semiconductor substrate including a plurality of
3 device structures thereon; and
4 an interconnect on the semiconductor substrate, the interconnect comprising at
5 least one slot provided in the semiconductor substrate and at least one metal within the slot.

1 17. The semiconductor device of claim 16 wherein the semiconductor substrate
2 comprises:
3 a substrate region; and a buried layer, or Boron Up Diffusion where required
4 and
5 an epitaxial (EPI) layer over the substrate region, wherein the device structures
6 are provided in the EPI layer.

1 18. The semiconductor device of claim 17 wherein the at least one metal comprises
2 a plurality of metals.

1 19. The semiconductor device of claim 18 wherein the plurality of metals comprises
2 two metals, a first metal covers one-half of the slot and a second metal fills the slot.

1 20. The semiconductor device of claim 19 wherein the plurality of metals comprises
2 three metal depositions, wherein the first and second deposition of metal fill the slot and a third
3 metal deposition provides the interconnect layer.

1 21. The semiconductor device of claim 16 wherein the at least one metal is provided
2 utilizing chemical vapor deposition.

1 22. The semiconductor device of claim 16 wherein the at least one metal is provided
2 utilizing sputter depositions.

1 23. A high current, high power interconnect on a semiconductor substrate
2 comprising:
3 at least one slot provided in the semiconductor substrate; and
4 at least one metal within the slot.

1 24. The high current, high power interconnect of claim 23 wherein the
2 semiconductor substrate comprises:

3 a substrate region; and
4 an epitaxial (EPI) layer over the substrate region, wherein the device structures
5 are provided in the EPI layer.

1 25. The high current interconnect of claim 24 with at least one metal comprises a
2 plurality of metals.

1 26. The high current interconnect of claim 25 wherein the plurality of metals
2 comprises two metals, a first meal covers one-half of the slot and a second metal fills the slot.

1 27. The high current interconnect of claim 25 wherein the plurality of metals
2 comprises three metals, wherein the first and second metal fill the slot and the third metal
3 provides an interconnect layer.

1 28. The high current interconnect of claim 23 wherein the at least one metal is
2 provided utilizing chemical vapor deposition.

1 29. The high current interconnect of claim 23 wherein the at least one metal is
2 provided utilizing sputter deposition.